1. A method of margin erasing memory cells in the testing procedure of a flash EPROM memory in an integrated circuit whereby said margin erasing uses the same charge pump circuitry to develop both the normal erase voltage used by the end user and the margin erase voltage.

2. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

3. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing series connected voltage dropping components.

4. The method according to Claim 3 whereby said series connected voltage dropping components are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.

5. The method according to Claim 3 whereby said series connected voltage dropping components are not bypassed during development of said normal erase voltage.

6. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected NMOS transistors.

7. The method according to Claim 6 whereby said plurality of diode-connected NMOS transistors is not bypassed during development of said normal erase voltage.

8. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected PMOS transistors.

9. The method according to Claim 8 whereby said plurality of diode-connected PMOS transistors is not bypassed during development of said normal erase voltage.

10. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of native NMOS transistors.

11. The method according to Claim 10 whereby said plurality of native NMOS transistors is not bypassed during development of said normal erase voltage.

12. The method according to Claim 1 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diodes.

13. The method according to Claim 12 whereby said plurality of diodes is not bypassed during development of said normal erase voltage.

14. A method of margin erasing memory cells in the testing procedure of a flash EPROM memory in an integrated circuit whereby said margin erasing uses the same internal charge pump circuit to develop both the normal erase voltage used by the end user and the margin erase voltage and whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

15. The method according to Claim 14 whereby said margin erase voltage is reduced by bypassing series connected voltage dropping components.

16. The method according to Claim 15 whereby said series connected voltage dropping components are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.

17. The method according to Claim 15 whereby said series connected voltage dropping components are not bypassed during development of said normal erase voltage.

18. The method according to Claim 14 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected NMOS transistors.

19. The method according to Claim 18 whereby said plurality of diode-connected NMOS transistors is not bypassed during development of said normal erase voltage.

20. The method according to Claim 14 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diode-connected PMOS transistors.

21. The method according to Claim 20 whereby said plurality of diode-connected PMOS transistors is not bypassed during development of said normal erase voltage.

22. The method according to Claim 14 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of native NMOS transistors.

23. The method according to Claim 22 whereby said plurality of native NMOS transistors is not bypassed during development of said normal erase voltage.

24. The method according to Claim 14 whereby said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage by bypassing a plurality of diodes.

25. The method according to Claim 24 whereby said plurality of diodes is not bypassed during development of said normal erase voltage.

26. A flash EPROM memory device comprising:

a charge pump circuit;

a protective diode whereby the cathode of said protective diode is connected to said charge pump circuit;

a plurality of series connected voltage dropping devices whereby the first of two terminals of said plurality of series connected voltage dropping devices is connected to the anode of said protective diode;

a bias current source connected to the second of two terminals of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices.

27. The method according to Claim 26 whereby said series connected voltage dropping devices are selected from the group consisting of: diode connected NMOS transistors, PMOS transistors, native NMOS transistors and diodes.